REMARKS/ARGUMENTS

Pending claims 1 and 9 stand rejected under 35 U.S.C. §102(e) over U.S. Patent Application No. 2003/0030729 (Prentice). Applicants respectfully traverse the rejection. With regard to claim 1, nowhere does Prentice disclose, at least, performing operations on image data produced in an imaging device. In this regard, it is telling that the Office Action can point to no specific portion of Prentice for such a teaching. Instead, Prentice merely discloses storing of image data in a RAM memory 34 and then transferring the stored image data to a host computer. For at least this reason, claims 1 and 9 are patentable over Prentice.

Pending claims 2-6, 16-22, 25-30 and 32 stand rejected under 35 U.S.C. §103(a) over Prentice. Applicants respectfully traverse the rejection. The Office Action takes Official Notice that it was known "to perform image processing techniques within the camera in order to decrease the complexity of the computer...". Office Action, pp. 3-4. Applicants respectfully traverse the Office Action's reliance on such Official Notice. MPEP §2144.03. This is especially so, as at the time of the invention, computers had more than sufficient capabilities to process image data, as shown in the cited references, including Prentice and U.S. Patent No. 6,269,181 (Acharya). Further, as shown in the attached exhibit obtained from the Intel Corporation website (www.intel.com), personal computers powered by microprocessors continue to operate faster, using more transistors, to handle more tasks, not less. *See* Exhibit A. Accordingly, the above-listed claims are patentable over Prentice for this further reason.

Dependent claim 6 is patentable for the further reason that nowhere does Prentice teach or suggest scaled color interpolation. Instead, Prentice merely teaches a spatial averaging of nearest neighbors. For this further reason, claim 6 and claims 7 and 8 depending therefrom are further patentable.

Independent claim 16 is patentable for similar reasons discussed above regarding claim 1. Further, as discussed above regarding dependent claim 2, there is no teaching or suggestion to combine Prentice with the asserted Official Notice to process image data in the imaging device and send uncompressed image data therefrom.

Dependent claim 26 is patentable for the further reason that nowhere does Prentice teach or suggest software to optionally perform color interpolation in either of two processor-based systems. Instead, the only color interpolation in Prentice is done in the host computer.

Claims 7, 8, 23, 24 and 31 stand rejected under 35 U.S.C. §103(a) over Prentice in view of Acharya. Applicants respectfully traverse the rejection. As discussed above, Prentice does not teach or suggest scaled color interpolation. Neither does Acharya. Instead, Acharya merely teaches replacing a missing pixel with a neighboring pixel based on a color median. In fact, Acharya teaches away from use of interpolation based on averaging. Acharya, col. 3, lns. 23-26; 35-39. Accordingly, for these further reasons, claims 7, 8, 23, 24 and 31 are further patentable over the proposed combination.

New dependent claims 33 and 34 are patentable at least for the same reasons discussed above regarding the independent claims from which they depend.

New claims 35-38 are patentable, at least because the cited references do not teach or suggest color interpolating before transferring processed image data if it is determined that a greater throughput is needed.

In view of these remarks, the application is now in condition for allowance and the Examiner's prompt action in accordance therewith is respectfully requested. The Commissioner is authorized to charge any additional fees or credit any overpayment to Deposit Account No. 20-1504.

Respectfully submitted,

Date: October 8, 2004

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Microprocessor Hall of Fame

Included on this page:

• 1970s Processors
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Technical Specifications

1970s Processors

	4004	8008	8080	8086	8088
Introduced	11/15/71	4/1/72	4/1/74	6/8/78	6/1/79
Clock Speeds	108KHz	200KHz	2MHz	5MHz, 8MHz, 10MHz	5MHz, 8MHz
Bus Width	4 bits	8 bits	8 bits	16 bits	8 bits
Number of Transistors	2,300 (10 microns)	3,500 (10 microns)	4.500 (6 microns)	29,000 (3 microns)	29,000 (3 microns)
Addressable Memory	640 bytes	16 KBytes	64 KBytes	1 MB	1 MB
Virtual Memory	--	--	--	--	--
Brief Description	First microcomputer chip, Arithmetic manipulation	Data/character manipulation	10X the performance of the 8008	10X the performance of the 8080	Identical to 8086 except for its 8-bit external bus

For more details check the Quick Reference Guide

1980s Processors

	80286	Intel386TM DX Microprocessor	Intel386TM SX Microprocessor	Intel486TM DX CPU Microprocessor
Introduced	2/1/82	10/17/85	6/16/88	4/10/89
Clock Speeds	6MHz, 8MHz, 10MHz, 12.5MHz	16MHz, 20MHz, 25MHz, 33MHz	16MHz, 20MHz, 25MHz, 33MHz	25MHz, 33MHz, 50MHz
Bus Width	16 bits	32 bits	16 bits	32 bits
Number of Transistors	134,000 (1.5 microns)	275,000 (1 micron)	275,000 (1 micron)	1.2 million (1 micron) (.8 micron with 50MHz)
Addressable Memory	16 megabytes	4 gigabytes	16 megabytes	4 gigabytes
Virtual Memory	1 gigabyte	64 terabytes	64 terabytes	64 terabytes
Brief Description	3-6X the performance of	First X86 chip to handle 32-bit data	16-bit address bus enabled low-cost 32-bit	Level 1 cache on chip

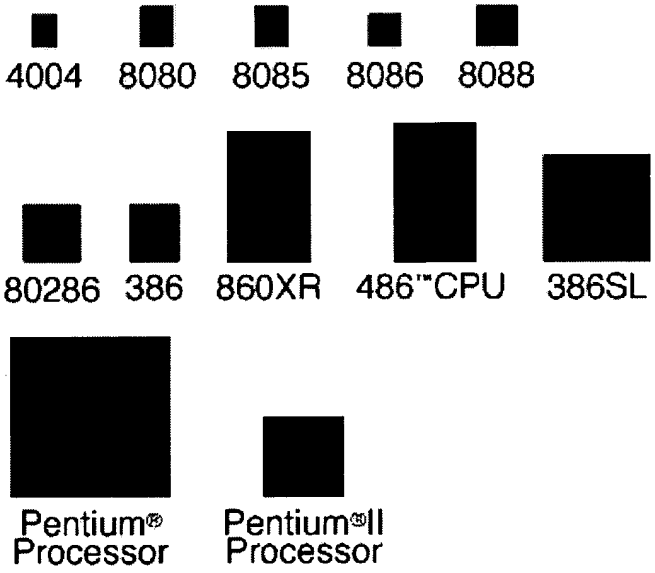
the 8086 sets processing

For more details check the Quick Reference Guide

1990s Processors

	Intel486TM SX Microprocessor	Pentium® Processor	Pentium® Pro Processor	Pentium® II Processor
Introduced	4/22/91	3/22/93	11/01/95	5/07/97
Clock Speeds	16MHz, 20MHz, 25MHz, 33MHz	60MHz,66MHz	150MHz, 166MHz, 180MHz, 200MHz	200MHz, 233MHz, 266MHz, 300MHz
Bus Width	32 bits	64 bits	64 bits	64 bits
Number of Transistors	1.185 million (1 micron)	3.1 million (.8 micron)	5.5 million (0.35 micron)	7.5 million (0.35 micron)
Addressable Memory	4 gigabytes	4 gigabytes	64 gigabytes	64 gigabytes
Virtual Memory	64 terabytes	64 terabytes	64 terabytes	64 terabytes
Brief Description	Identical in design to Intel486™ DX but without math coprocessor	Superscalar architecture brought 5X the performance of the 33-MHz Intel486™ DX processor	Dynamic execution architecture drives high-performing processor	Dual independent bus, dynamic execution, Intel MMX™ technology
Other Processor Family Members	Quick Reference Guide	Quick Reference Guide	Quick Reference Guide	Quick Reference Guide

Approximate Size Relationship



For more details check the Quick Reference Guide

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